FIG.1

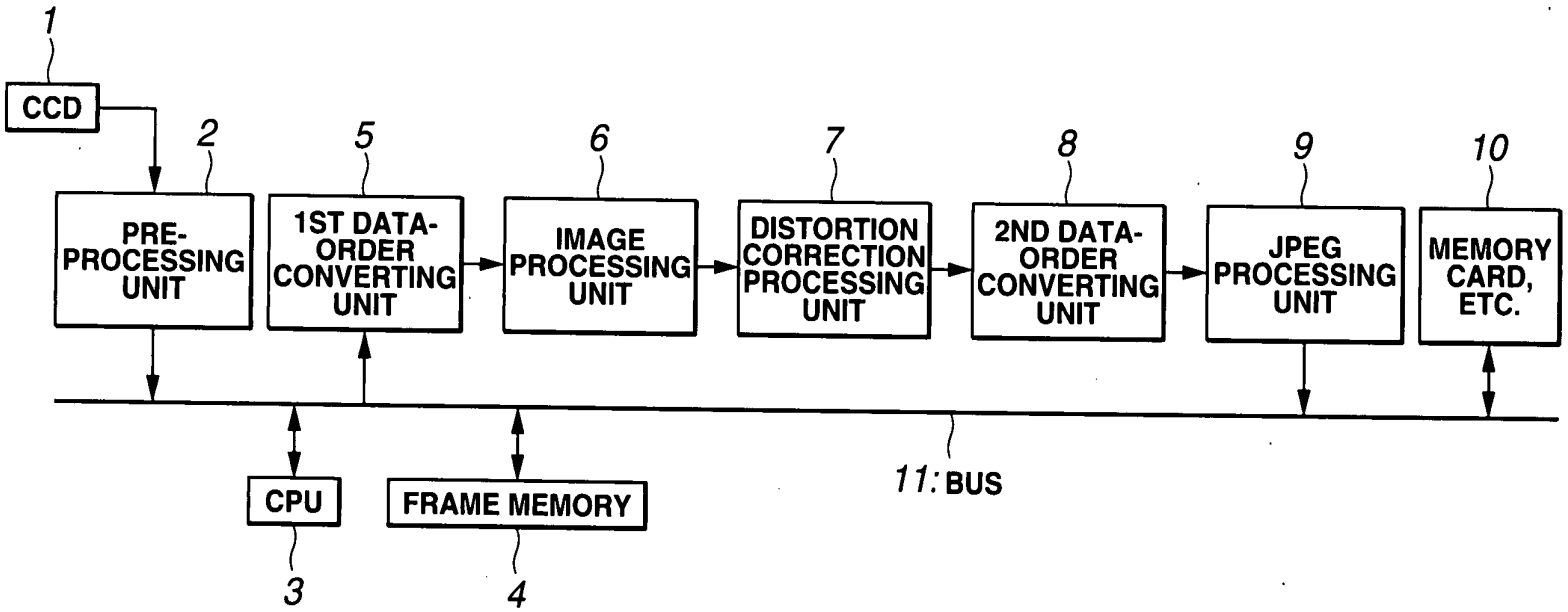

1
CCD
2
PRE-PROCESSING UNIT
5
1ST DATA-ORDER CONVERTING UNIT
6
IMAGE PROCESSING UNIT
7
DISTORTION CORRECTION PROCESSING UNIT
8
2ND DATA-ORDER CONVERTING UNIT
9
JPEG PROCESSING UNIT
10
MEMORY CARD, ETC.
11: BUS
CPU
3
FRAME MEMORY
4

FIG.2

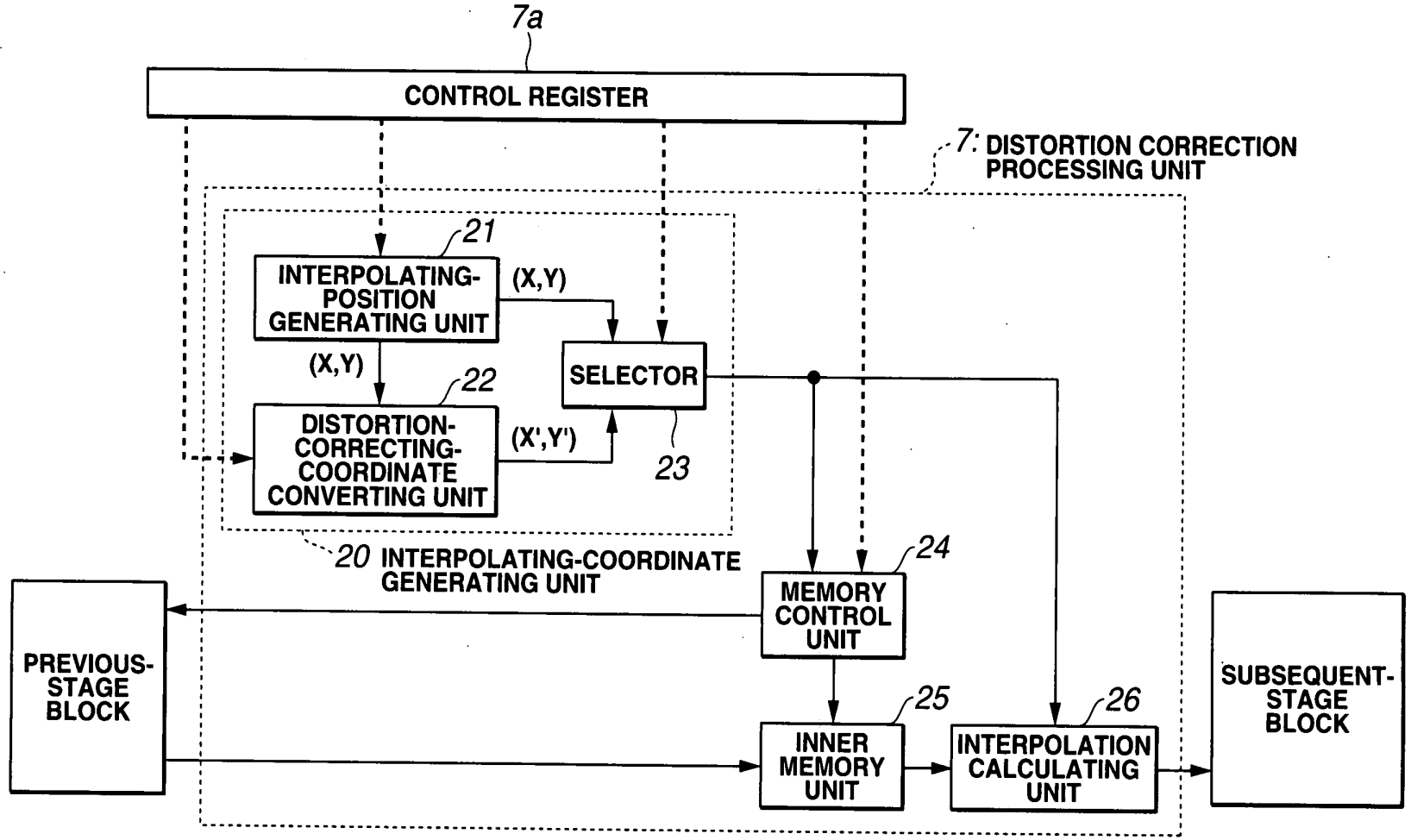

7a
CONTROL REGISTER
7: DISTORTION CORRECTION PROCESSING UNIT
21
INTERPOLATING-POSITION GENERATING UNIT
(X,Y)
(X,Y)
22
DISTORTION-CORRECTING-COORDINATE CONVERTING UNIT
(X',Y')
SELECTOR
23
20 INTERPOLATING-COORDINATE GENERATING UNIT
24
MEMORY CONTROL UNIT
PREVIOUS-STAGE BLOCK
25
INNER MEMORY UNIT
26
INTERPOLATION CALCULATING UNIT
SUBSEQUENT-STAGE BLOCK

FIG.3A

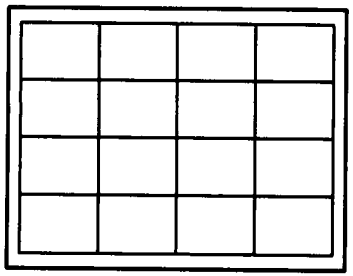


FIG.3B

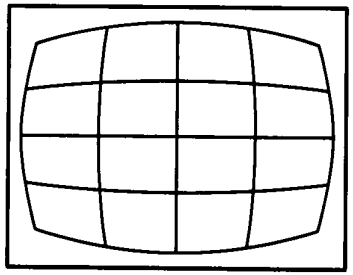


FIG.3C

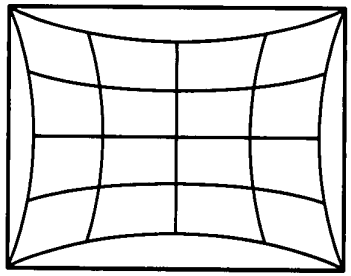


FIG.3D

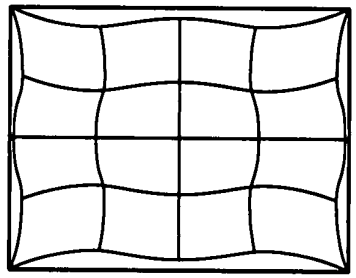
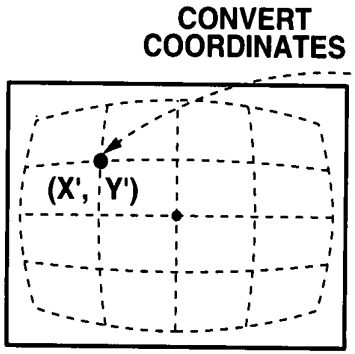


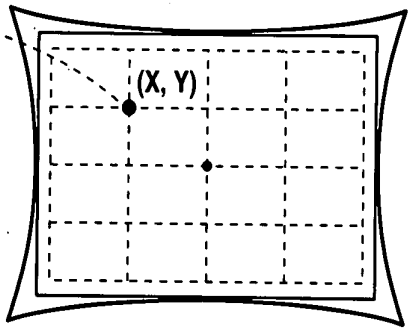
FIG.4A



CAPTURED IMAGE DATA

FIG.4B

CONVERT COORDINATES



CORRECTED IMAGE

FIG.5

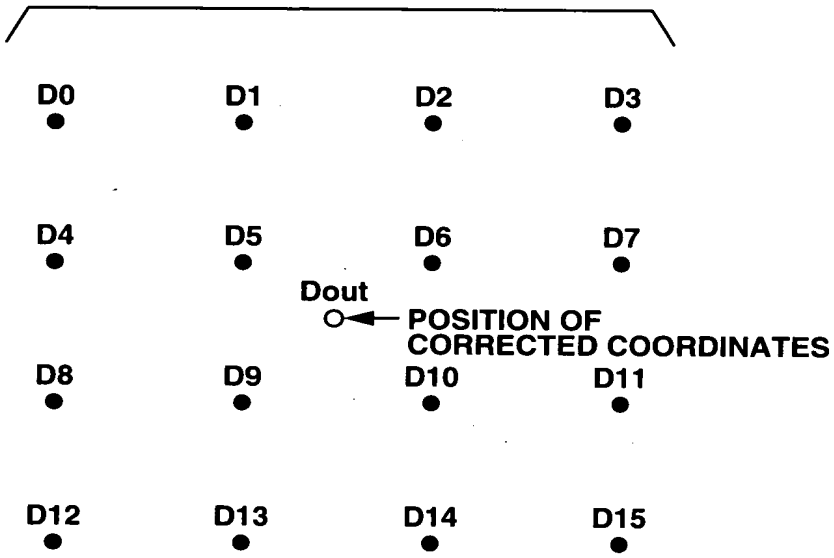

D0
D1
D2
D3
D4
D5
D6
D7
Dout
POSITION OF
CORRECTED COORDINATES
D8
D9
D10
D11
D12
D13
D14
D15

FIG.6

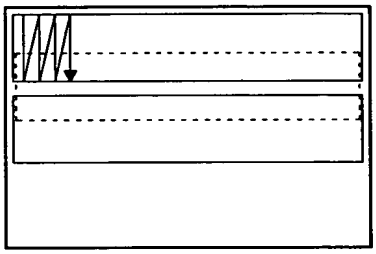


FIG.7A

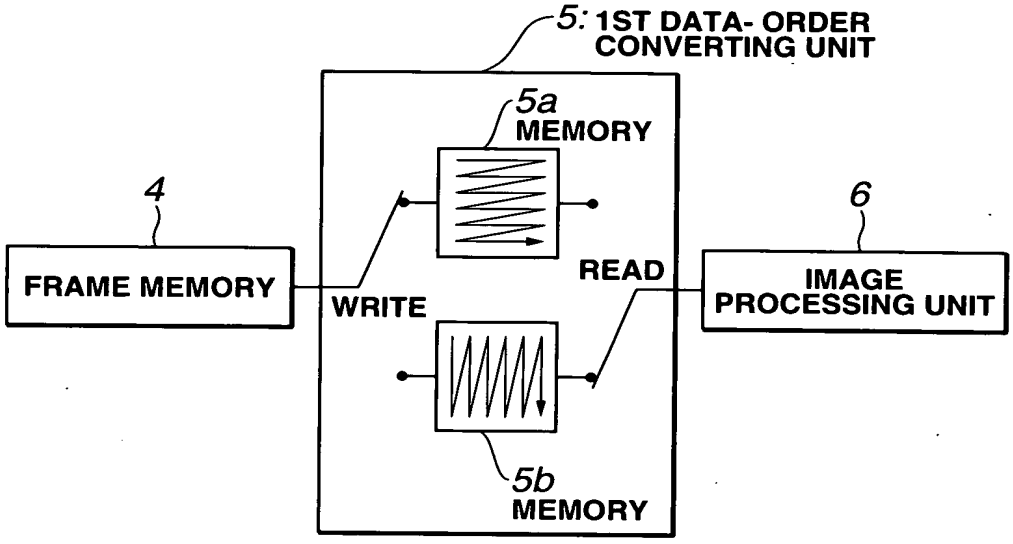

5: 1ST DATA- ORDER CONVERTING UNIT
5a MEMORY
4
FRAME MEMORY
WRITE
READ
6
IMAGE PROCESSING UNIT
5b MEMORY

FIG.7B

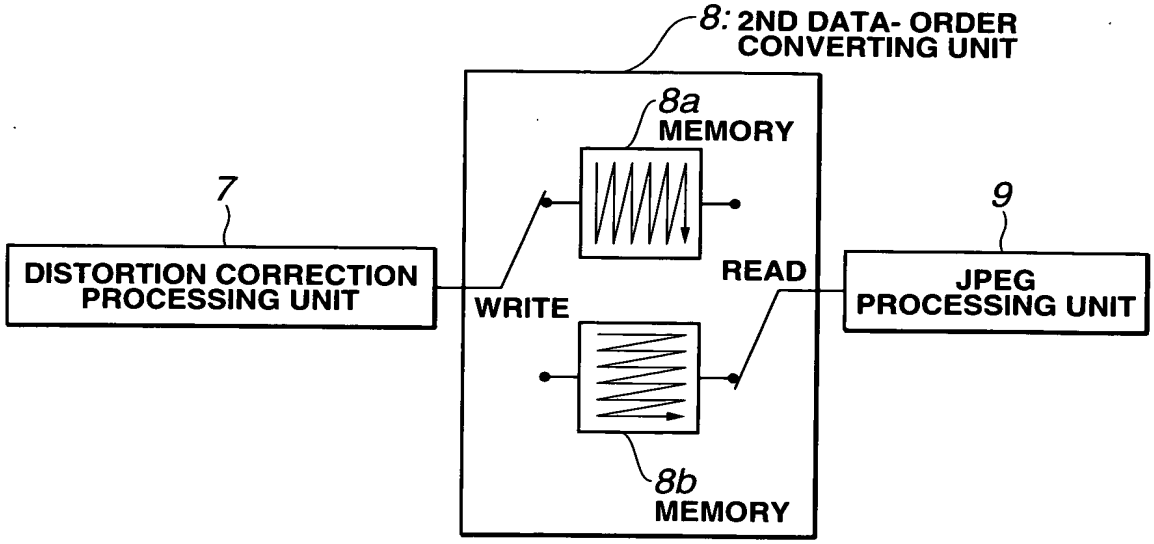

8: 2ND DATA- ORDER CONVERTING UNIT
8a MEMORY
7
DISTORTION CORRECTION PROCESSING UNIT
WRITE
READ
9
JPEG PROCESSING UNIT
8b MEMORY

FIG.8

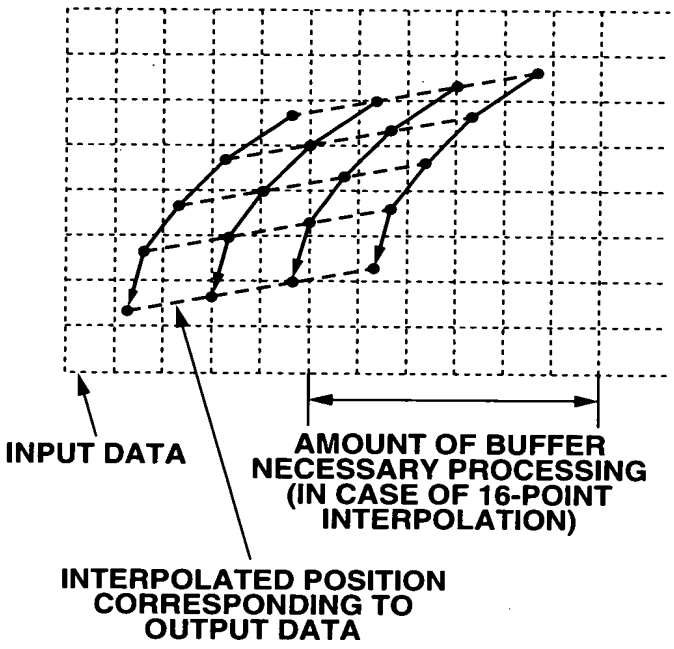

INPUT DATA
AMOUNT OF BUFFER NECESSARY PROCESSING (IN CASE OF 16-POINT INTERPOLATION)
INTERPOLATED POSITION CORRESPONDING TO OUTPUT DATA

FIG.9

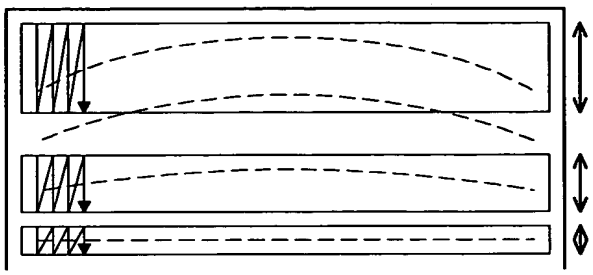


FIG.10

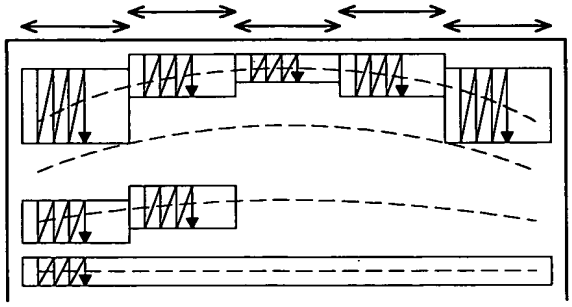


FIG.11

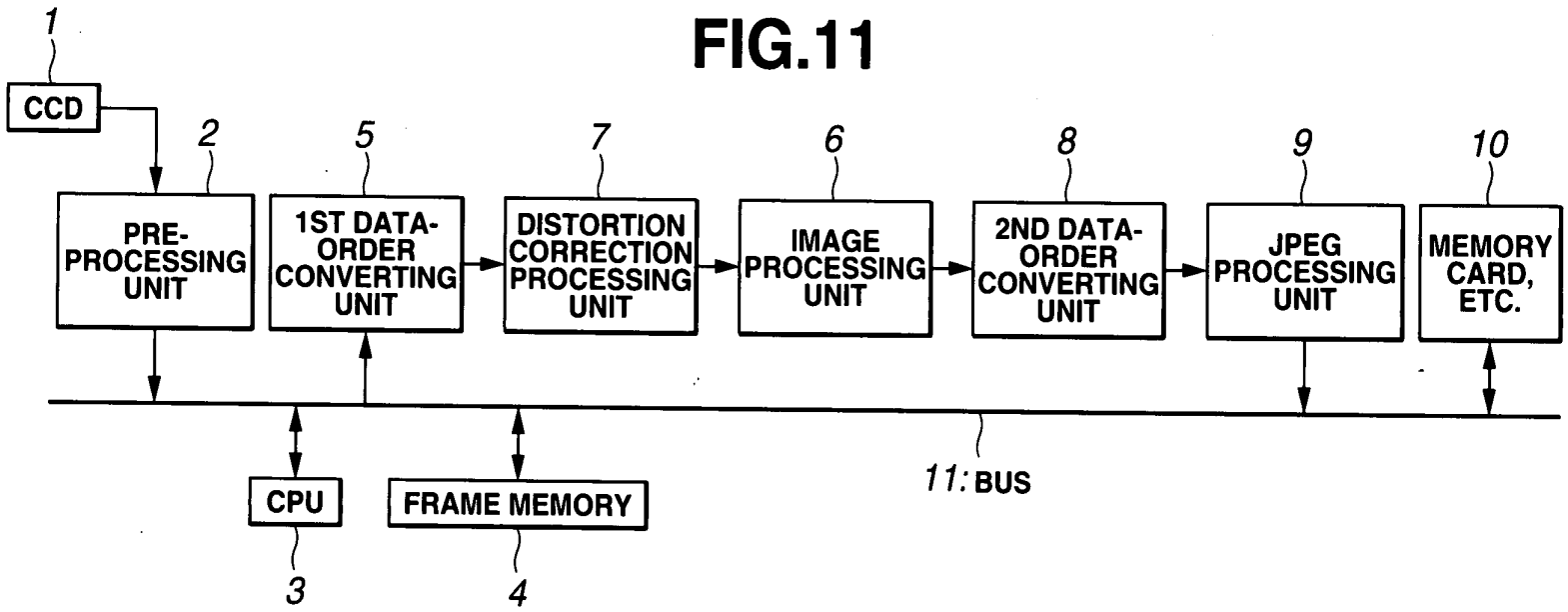

1
CCD
2
PRE-PROCESSING UNIT
5
1ST DATA-ORDER CONVERTING UNIT
7
DISTORTION CORRECTION PROCESSING UNIT
6
IMAGE PROCESSING UNIT
8
2ND DATA-ORDER CONVERTING UNIT
9
JPEG PROCESSING UNIT
10
MEMORY CARD, ETC.
11: BUS
CPU
3
FRAME MEMORY
4

FIG.12

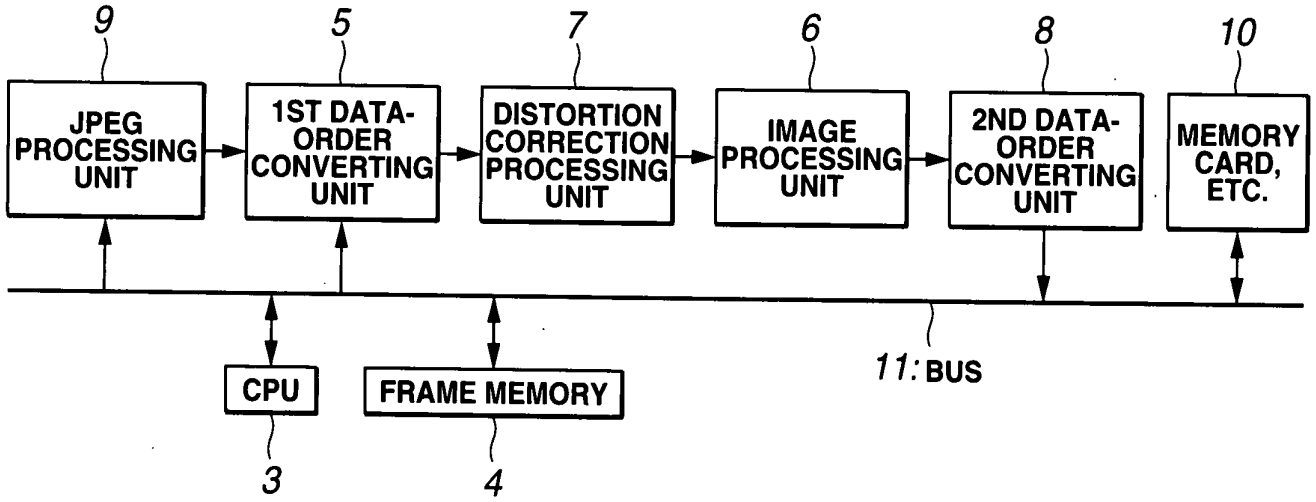

9
JPEG PROCESSING UNIT
5
1ST DATA-ORDER CONVERTING UNIT
7
DISTORTION CORRECTION PROCESSING UNIT
6
IMAGE PROCESSING UNIT
8
2ND DATA-ORDER CONVERTING UNIT
10
MEMORY CARD, ETC.
11: BUS
CPU
3
FRAME MEMORY
4

FIG.13

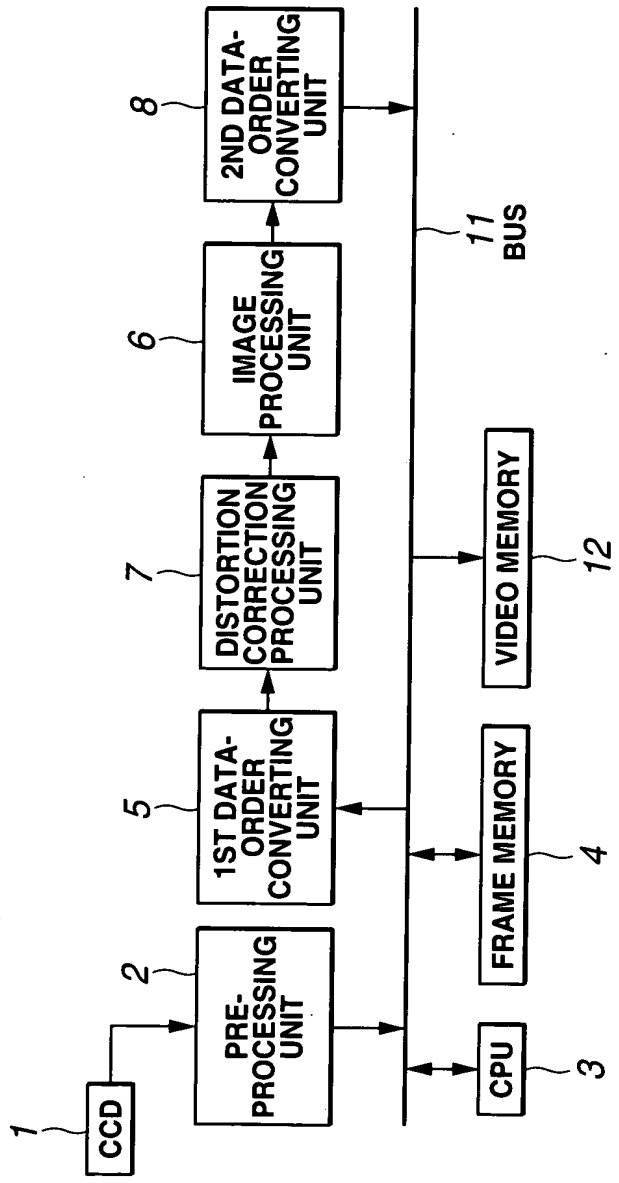

1
CCD
2
PRE-PROCESSING UNIT
5
1ST DATA-ORDER CONVERTING UNIT
7
DISTORTION CORRECTION PROCESSING UNIT
6
IMAGE PROCESSING UNIT
8
2ND DATA-ORDER CONVERTING UNIT
11
BUS
3
CPU
4
FRAME MEMORY
12
VIDEO MEMORY

FIG.14

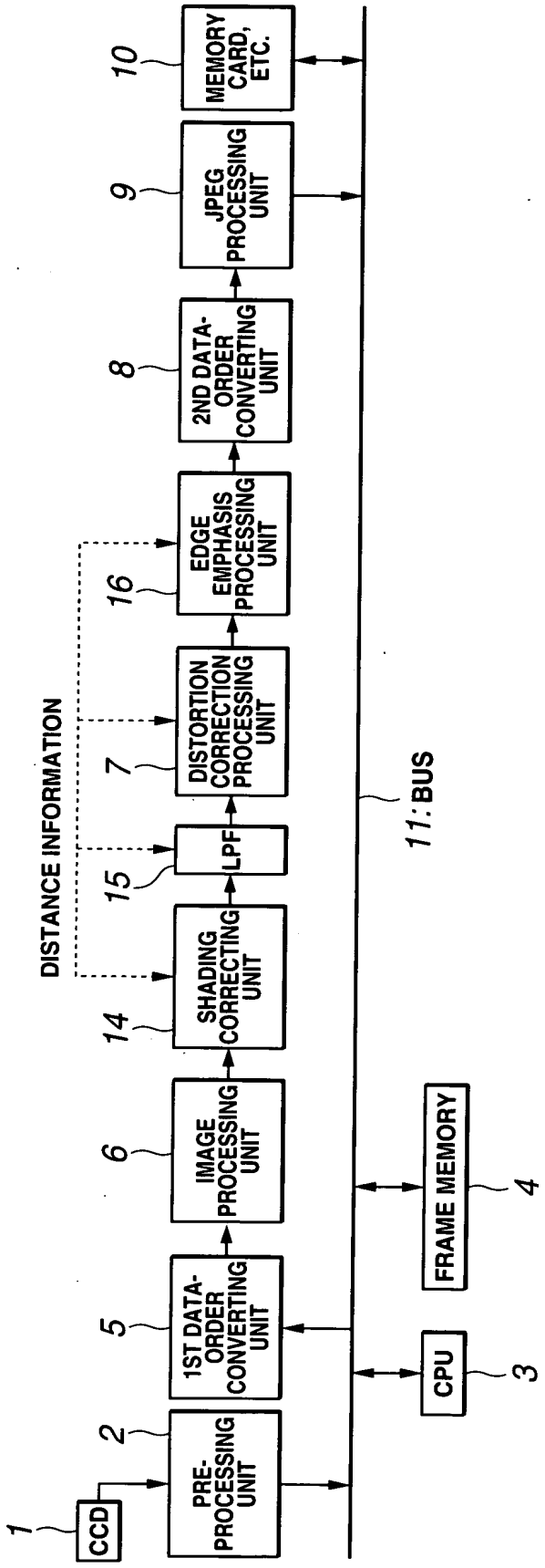

1
CCD
PRE-PROCESSING UNIT
2
1ST DATA-ORDER CONVERTING UNIT
5
IMAGE PROCESSING UNIT
6
SHADING CORRECTING UNIT
14
LPF
15
DISTORTION CORRECTION PROCESSING UNIT
7
EDGE EMPHASIS PROCESSING UNIT
16
2ND DATA-ORDER CONVERTING UNIT
8
JPEG PROCESSING UNIT
9
MEMORY CARD, ETC.
10
DISTANCE INFORMATION
11: BUS
CPU
3
FRAME MEMORY
4

FIG.15

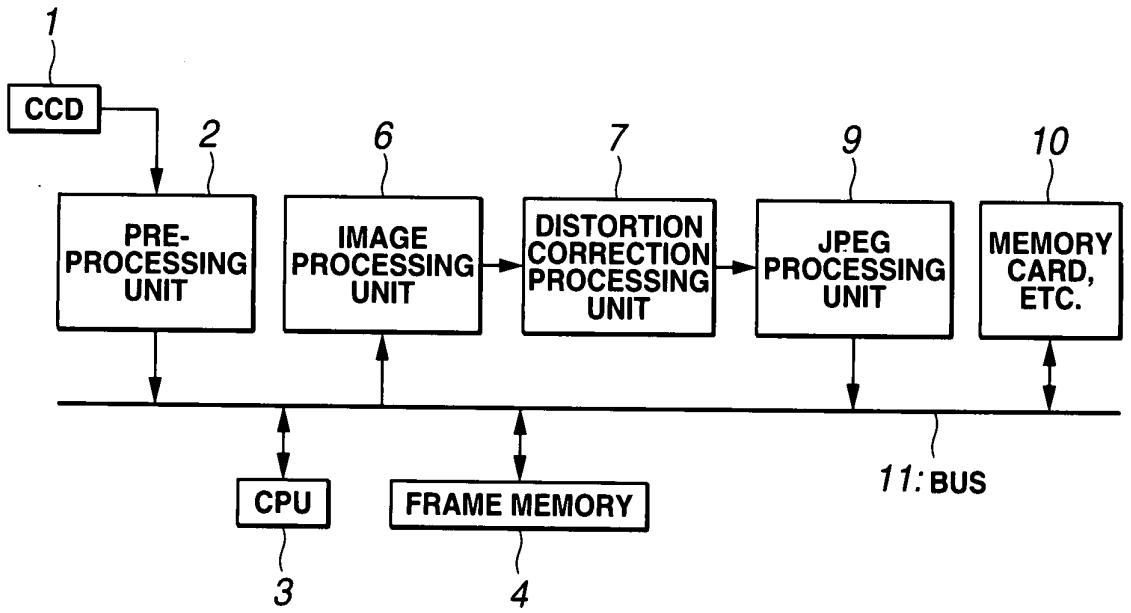

1
CCD
2
PRE-PROCESSING UNIT
6
IMAGE PROCESSING UNIT
7
DISTORTION CORRECTION PROCESSING UNIT
9
JPEG PROCESSING UNIT
10
MEMORY CARD, ETC.
CPU
3
FRAME MEMORY
4
11: BUS

FIG.16

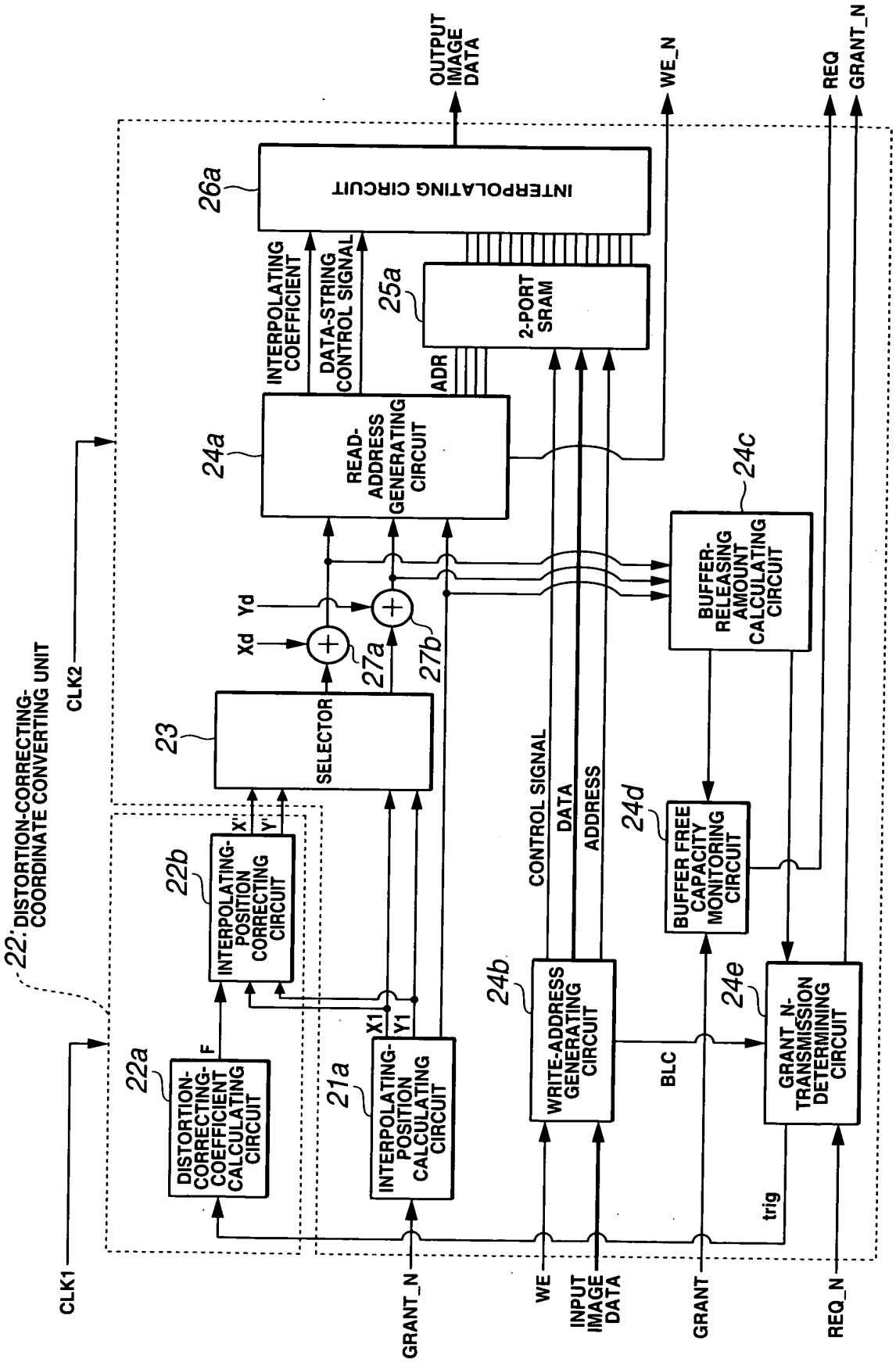

22: DISTORTION-CORRECTING-COORDINATE CONVERTING UNIT
CLK1
CLK2
22a
DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
F
22b
INTERPOLATING-POSITION CORRECTING CIRCUIT
X'
Y'
21a
INTERPOLATING-POSITION CALCULATING CIRCUIT
X1
Y1
23
SELECTOR
Xd
Yd
27a
27b
24a
READ-ADDRESS GENERATING CIRCUIT
INTERPOLATING COEFFICIENT
DATA-STRING CONTROL SIGNAL
ADR
25a
2-PORT SRAM
26a
INTERPOLATING CIRCUIT
OUTPUT IMAGE DATA
WE_N
REQ
GRANT_N
24b
WRITE-ADDRESS GENERATING CIRCUIT
CONTROL SIGNAL
DATA
ADDRESS
BLC
24c
BUFFER-RELEASING AMOUNT CALCULATING CIRCUIT
24d
BUFFER FREE CAPACITY MONITORING CIRCUIT
24e
GRANT_N-TRANSMISSION DETERMINING CIRCUIT
trig
GRANT_N
WE
INPUT IMAGE DATA
GRANT
REQ_N

FIG.17

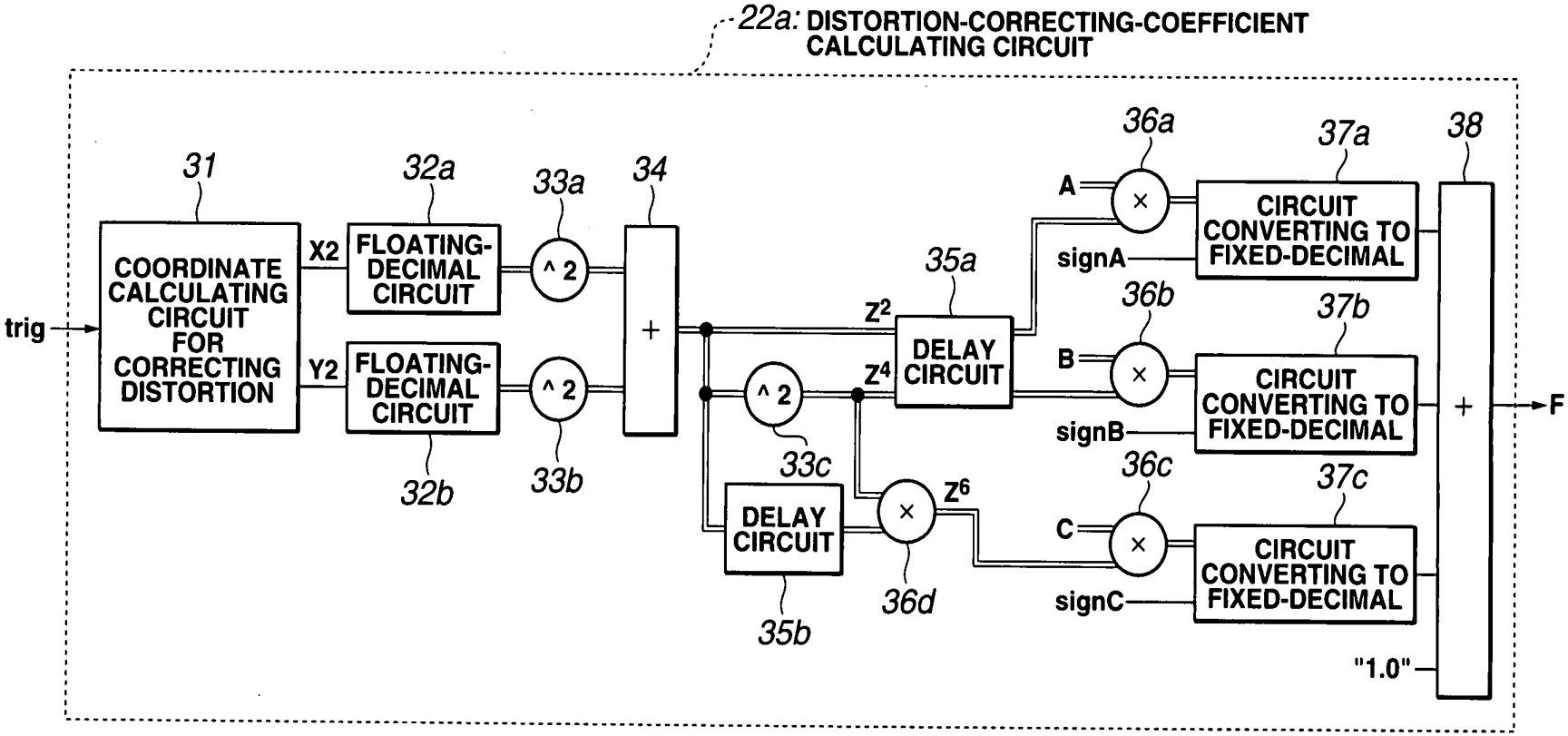

22a: DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
31
COORDINATE CALCULATING CIRCUIT FOR CORRECTING DISTORTION
trig
X2
Y2
32a
FLOATING-DECIMAL CIRCUIT
32b
FLOATING-DECIMAL CIRCUIT
33a
^ 2
33b
^ 2
34
+
35a
DELAY CIRCUIT
Z2
Z4
^ 2
33c
35b
DELAY CIRCUIT
Z6
36d
36a
A
signA
CIRCUIT CONVERTING TO FIXED-DECIMAL
37a
36b
B
signB
CIRCUIT CONVERTING TO FIXED-DECIMAL
37b
36c
C
signC
CIRCUIT CONVERTING TO FIXED-DECIMAL
37c
"1.0"
38
+
F

FIG.18

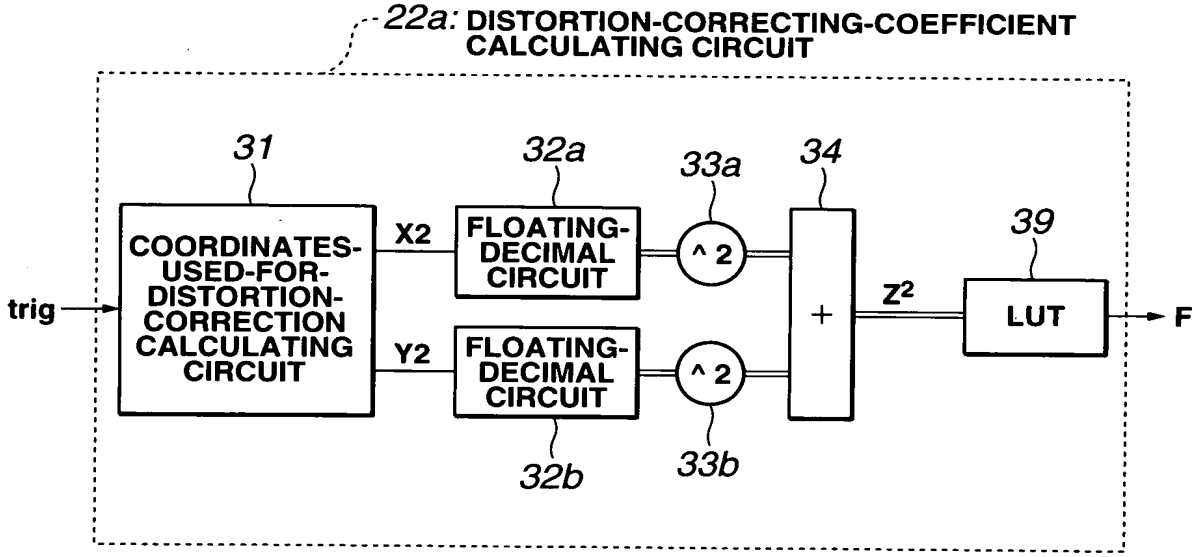

22a: DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
31
32a
33a
34
39
COORDINATES-USED-FOR-DISTORTION-CORRECTION CALCULATING CIRCUIT
X2
FLOATING-DECIMAL CIRCUIT
^ 2
trig
Y2
FLOATING-DECIMAL CIRCUIT
^ 2
+
Z²
LUT
F
32b
33b

FIG.19

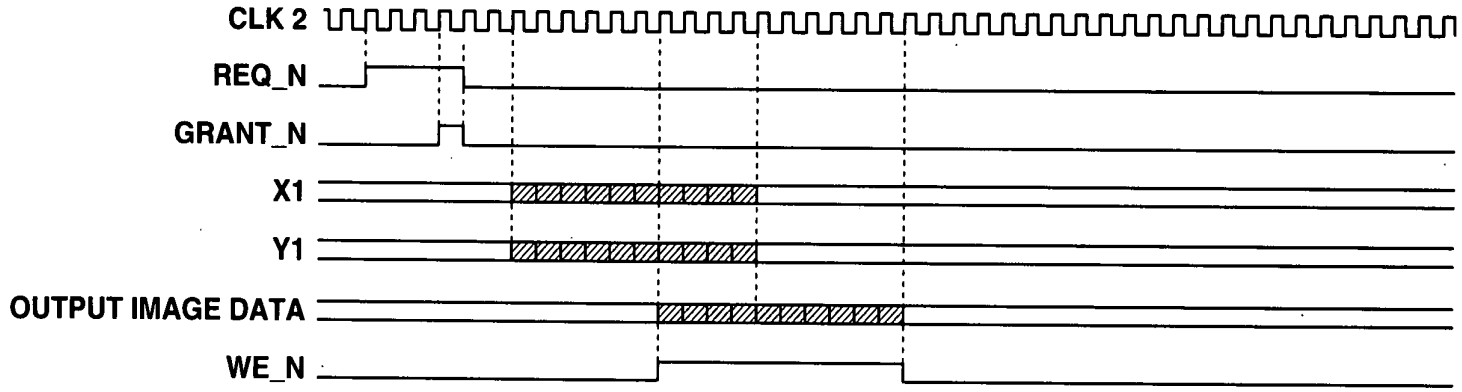

CLK 2
REQ_N
GRANT_N
X1
Y1
OUTPUT IMAGE DATA
WE_N

FIG.20

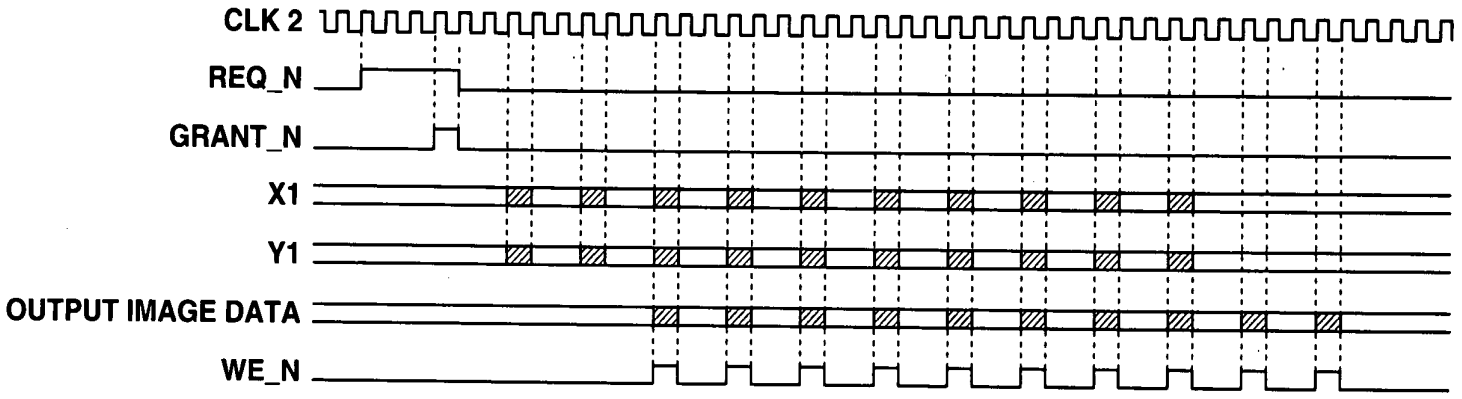

CLK 2
REQ_N
GRANT_N
X1
Y1
OUTPUT IMAGE DATA
WE_N

FIG.21

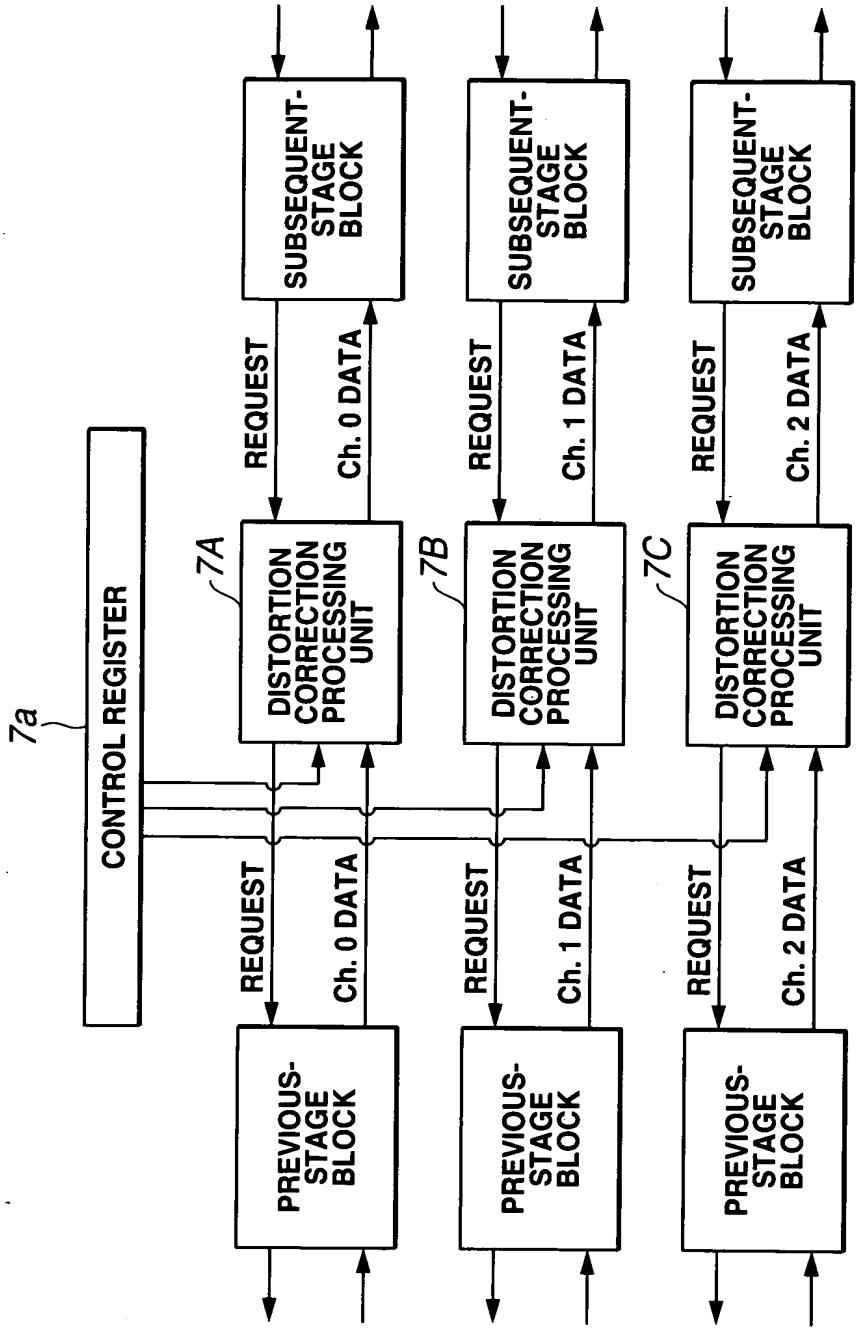

7a
CONTROL REGISTER
7A
7B
7C
DISTORTION CORRECTION PROCESSING UNIT
DISTORTION CORRECTION PROCESSING UNIT
DISTORTION CORRECTION PROCESSING UNIT
REQUEST
Ch. 0 DATA
REQUEST
Ch. 1 DATA
REQUEST
Ch. 2 DATA
SUBSEQUENT-STAGE BLOCK
SUBSEQUENT-STAGE BLOCK
SUBSEQUENT-STAGE BLOCK
REQUEST
Ch. 0 DATA
REQUEST
Ch. 1 DATA
REQUEST
Ch. 2 DATA
PREVIOUS-STAGE BLOCK
PREVIOUS-STAGE BLOCK
PREVIOUS-STAGE BLOCK

FIG.22

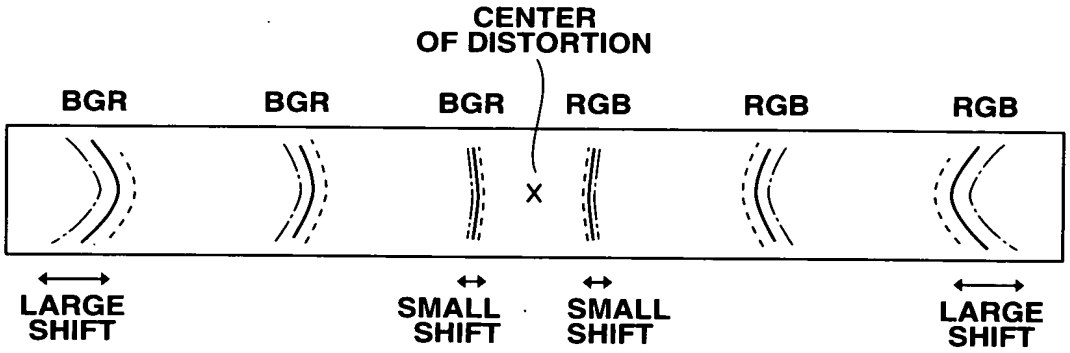

CENTER
OF DISTORTION
BGR
BGR
BGR
RGB
RGB
RGB
X
LARGE
SHIFT
SMALL
SHIFT
SMALL
SHIFT
LARGE
SHIFT

FIG.23A

FIG.23B

FIG.23C

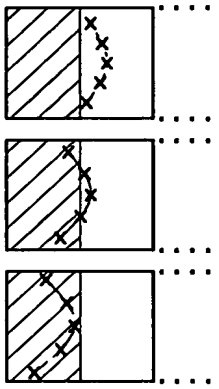


FIG.24A

FIG.24B

FIG.24C

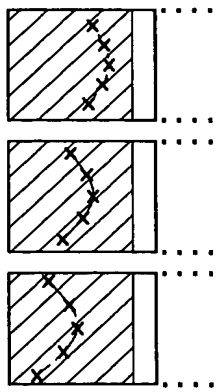


FIG.25

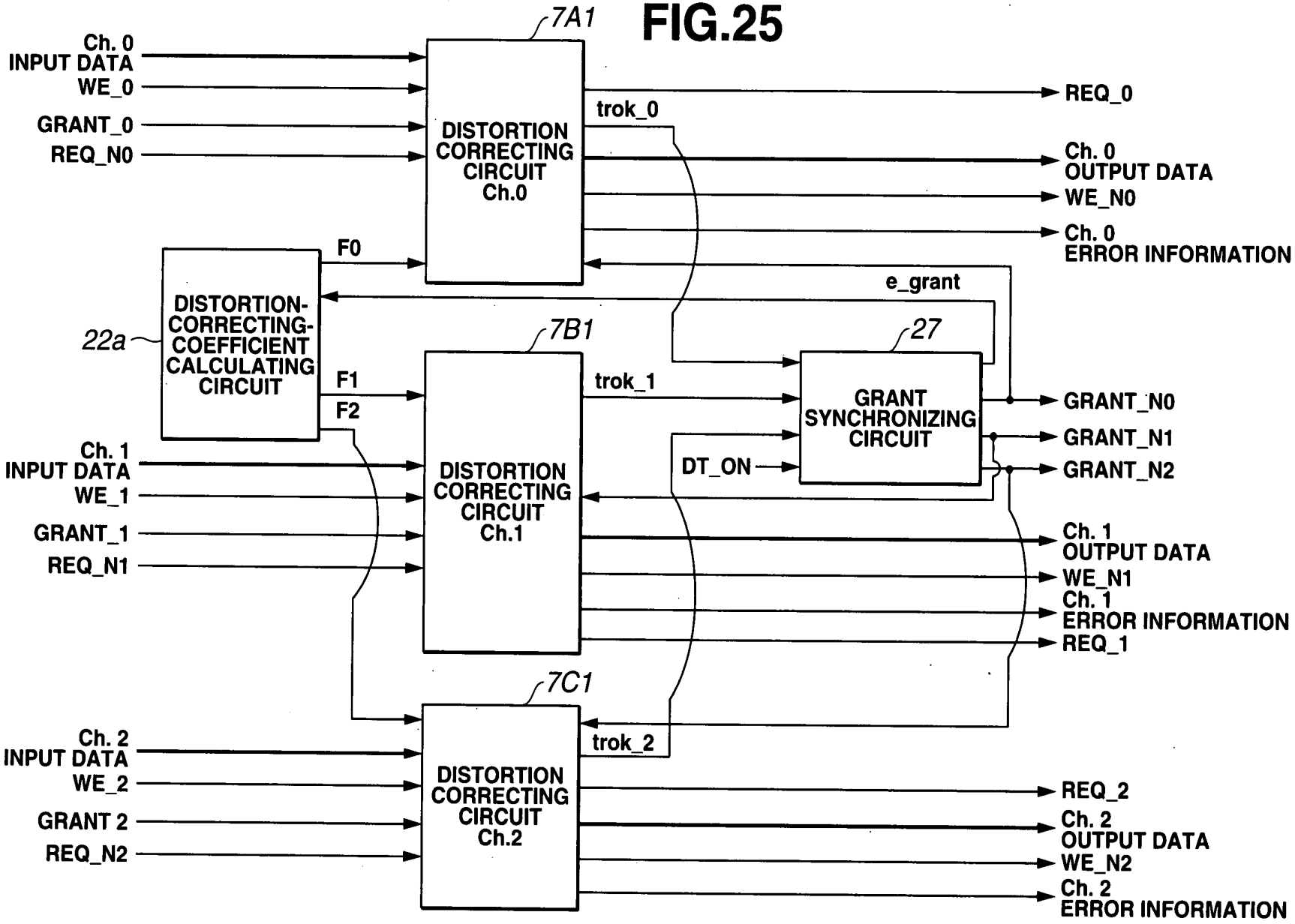

7A1
Ch. 0
INPUT DATA
WE_0
GRANT_0
REQ_N0
DISTORTION CORRECTING CIRCUIT Ch.0
trok_0
REQ_0
Ch. 0
OUTPUT DATA
WE_N0
Ch. 0
ERROR INFORMATION
F0
e_grant
22a
DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
7B1
27
F1
F2
trok_1
GRANT SYNCHRONIZING CIRCUIT
GRANT_N0
GRANT_N1
GRANT_N2
DT_ON
Ch. 1
INPUT DATA
WE_1
GRANT_1
REQ_N1
DISTORTION CORRECTING CIRCUIT Ch.1
Ch. 1
OUTPUT DATA
WE_N1
Ch. 1
ERROR INFORMATION
REQ_1
7C1
trok_2
Ch. 2
INPUT DATA
WE_2
GRANT 2
REQ_N2
DISTORTION CORRECTING CIRCUIT Ch.2
REQ_2
Ch. 2
OUTPUT DATA
WE_N2
Ch. 2
ERROR INFORMATION

FIG.26

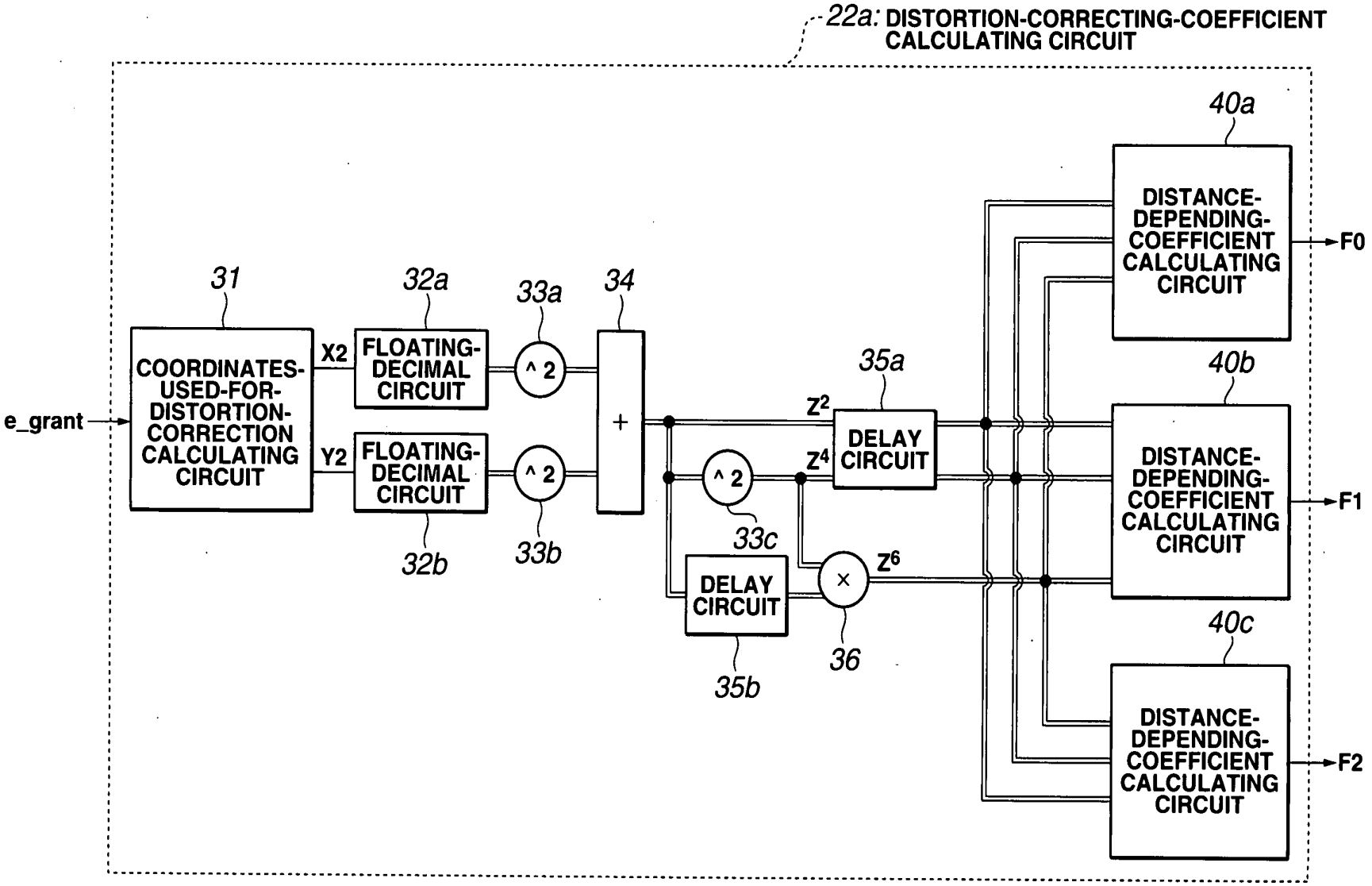

22a: DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
e_grant
31
COORDINATES-USED-FOR-DISTORTION-CORRECTION CALCULATING CIRCUIT
X2
Y2
32a
FLOATING-DECIMAL CIRCUIT
32b
FLOATING-DECIMAL CIRCUIT
33a
^ 2
33b
^ 2
34
+
35a
DELAY CIRCUIT
Z2
Z4
^ 2
33c
DELAY CIRCUIT
35b
Z6
×
36
40a
DISTANCE-DEPENDING-COEFFICIENT CALCULATING CIRCUIT
F0
40b
DISTANCE-DEPENDING-COEFFICIENT CALCULATING CIRCUIT
F1
40c
DISTANCE-DEPENDING-COEFFICIENT CALCULATING CIRCUIT
F2

FIG.27

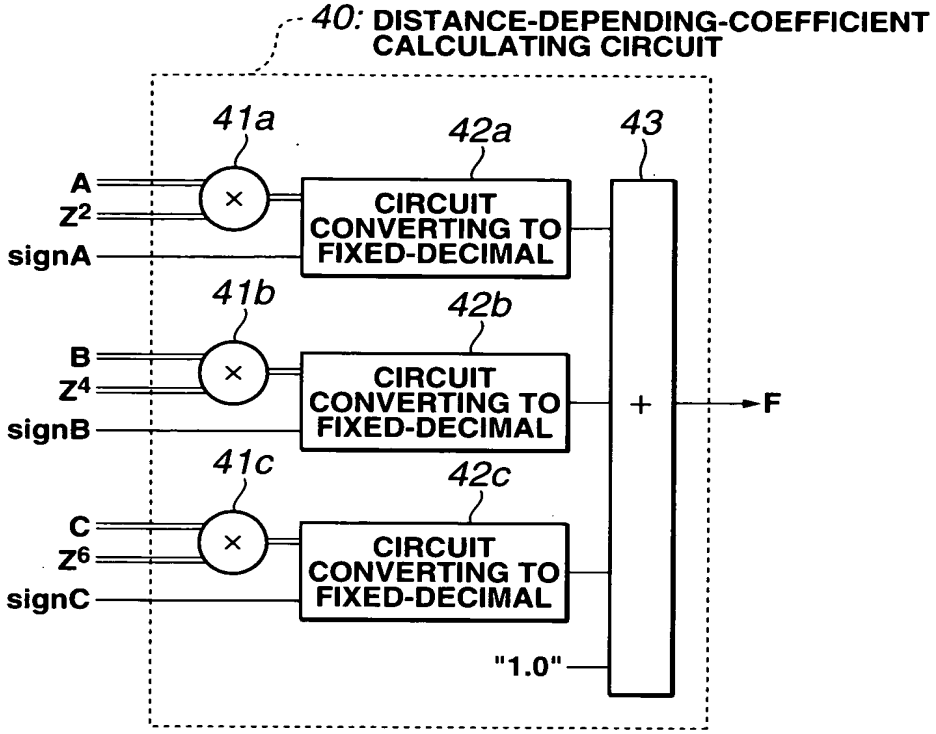

40: DISTANCE-DEPENDING-COEFFICIENT CALCULATING CIRCUIT
41a
42a
43
A
Z2
signA
CIRCUIT CONVERTING TO FIXED-DECIMAL
41b
42b
B
Z4
signB
CIRCUIT CONVERTING TO FIXED-DECIMAL
F
41c
42c
C
Z6
signC
CIRCUIT CONVERTING TO FIXED-DECIMAL
"1.0"

FIG.28

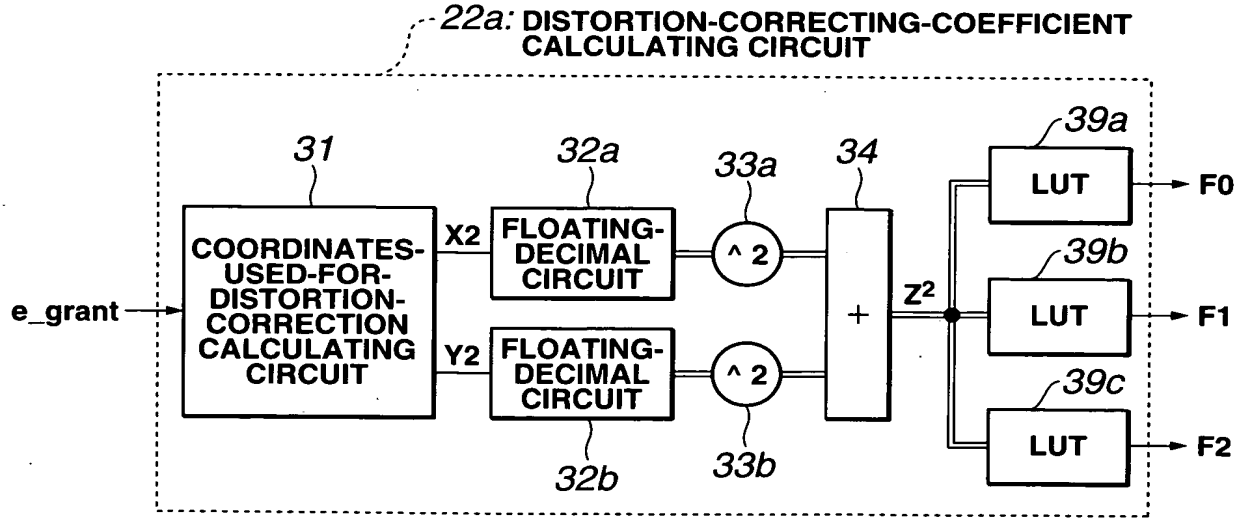

22a: DISTORTION-CORRECTING-COEFFICIENT CALCULATING CIRCUIT
31
32a
33a
34
39a
LUT
F0
e_grant
COORDINATES-USED-FOR-DISTORTION-CORRECTION CALCULATING CIRCUIT
X2
FLOATING-DECIMAL CIRCUIT
^ 2
Z2
39b
LUT
F1
Y2
FLOATING-DECIMAL CIRCUIT
^ 2
39c
LUT
F2
32b
33b

FIG.29

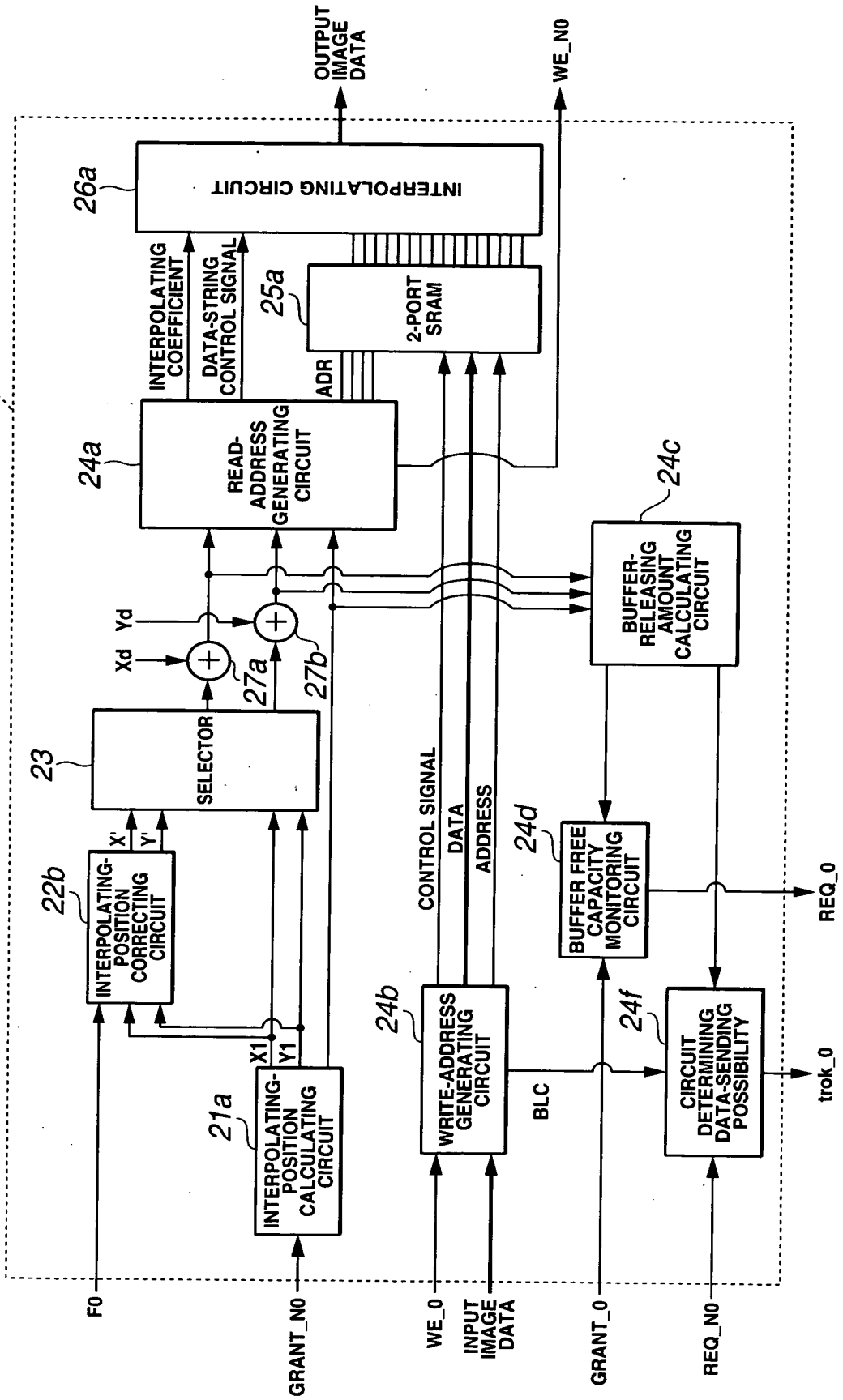

7A1: DISTORTION CORRECTING CIRCUIT FOR Ch. 0
OUTPUT IMAGE DATA
WE_N0
26a
INTERPOLATING CIRCUIT
INTERPOLATING COEFFICIENT
DATA-STRING CONTROL SIGNAL
25a
2-PORT SRAM
ADR
24a
READ-ADDRESS GENERATING CIRCUIT
24c
BUFFER-RELEASING AMOUNT CALCULATING CIRCUIT
Xd
Yd
27a
27b
23
SELECTOR
X'
Y'
22b
INTERPOLATING-POSITION CORRECTING CIRCUIT
X1
Y1
21a
INTERPOLATING-POSITION CALCULATING CIRCUIT
CONTROL SIGNAL
DATA
ADDRESS
24b
WRITE-ADDRESS GENERATING CIRCUIT
BLC
24d
BUFFER FREE CAPACITY MONITORING CIRCUIT
REQ_0
24f
CIRCUIT DETERMINING DATA-SENDING POSSIBILITY
trok_0
F0
GRANT_N0
WE_0
INPUT IMAGE DATA
GRANT_0
REQ_N0

FIG.30

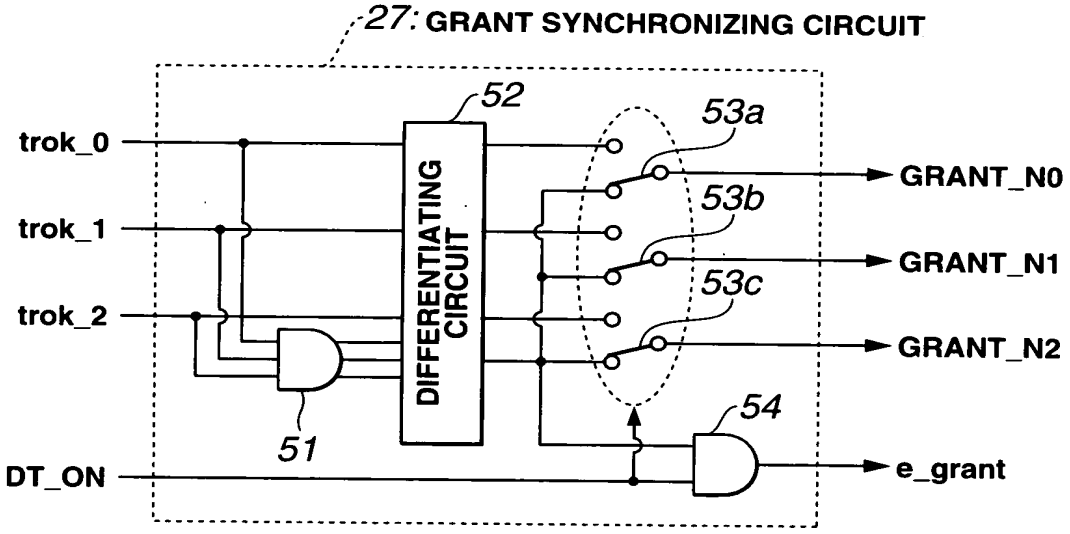

27: GRANT SYNCHRONIZING CIRCUIT
52
53a
53b
53c
54
51
trok_0
trok_1
trok_2
DT_ON
DIFFERENTIATING CIRCUIT
GRANT_N0
GRANT_N1
GRANT_N2
e_grant

FIG.31

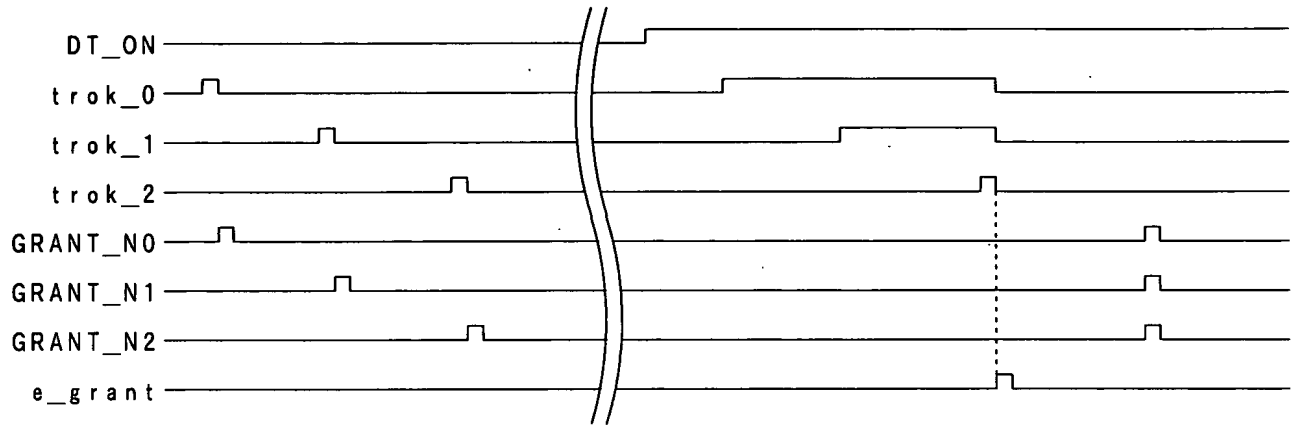


FIG.32

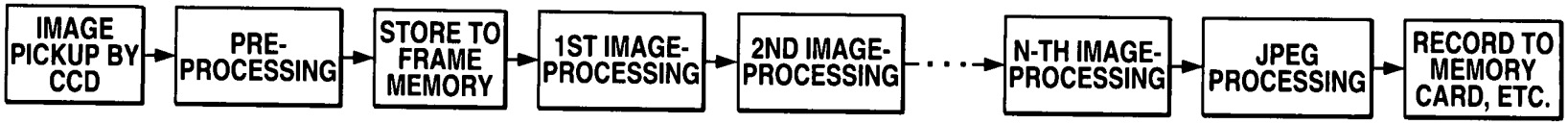
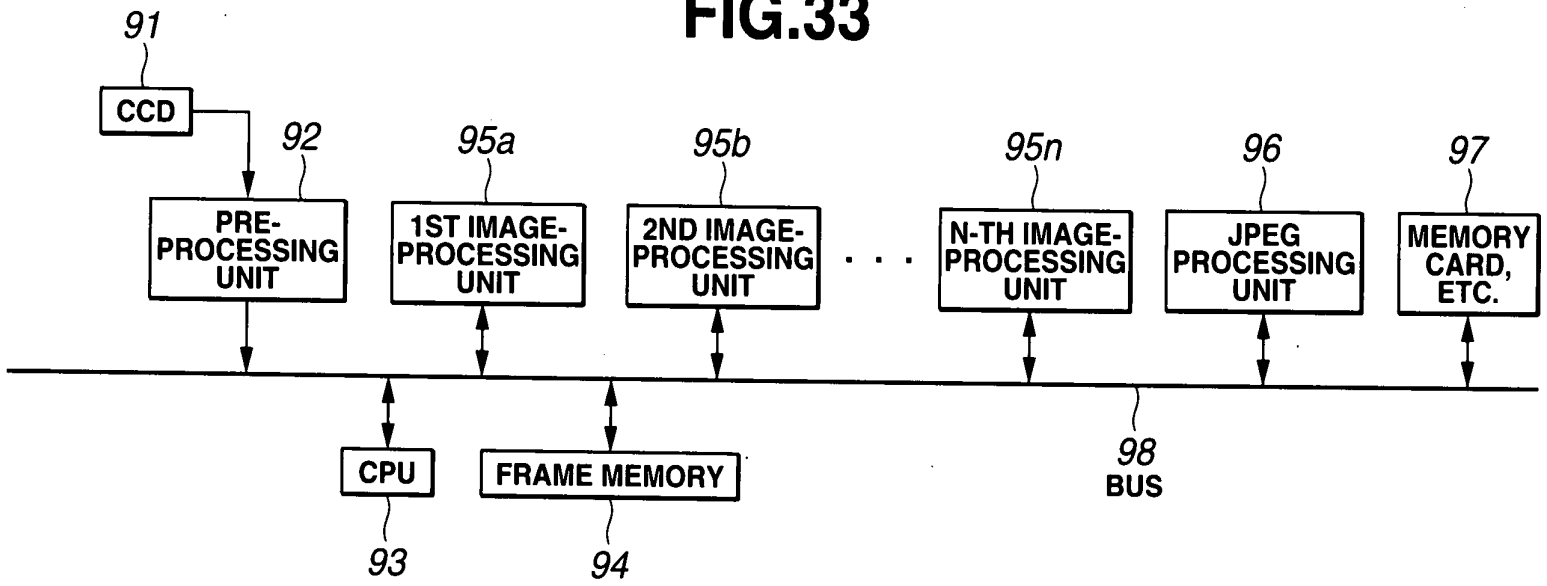


IMAGE PICKUP BY CCD
PRE-PROCESSING
STORE TO FRAME MEMORY
1ST IMAGE-PROCESSING
2ND IMAGE-PROCESSING
N-TH IMAGE-PROCESSING
JPEG PROCESSING
RECORD TO MEMORY CARD, ETC.

FIG.33


91
CCD
92
PRE-PROCESSING UNIT
95a
1ST IMAGE-PROCESSING UNIT
95b
2ND IMAGE-PROCESSING UNIT
95n
N-TH IMAGE-PROCESSING UNIT
96
JPEG PROCESSING UNIT
97
MEMORY CARD, ETC.
CPU
93
FRAME MEMORY
94
98
BUS

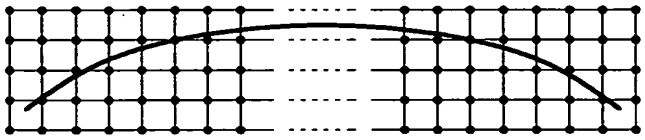



FIG.34